Kuldeep Gohil

015499534

John Tramel

Project 6 Report

**Description**: In this project, the main goal was to see how a sequential specific flop works, but because the NEXYS board has 100Mhz of frequency, the period of it was at 10ns, something very hard to notice happening fast on small LEDs.

**What I Have Done:** In this project, I first wrote a Verilog for a D-Flop. This had the inputs clk, reset, and D in it and the output Q in it. Then I wrote a Verilog for a 8-bit register to be added with the D-Flop. Then I wrote a Verilog of a Loadable 8-bit Register to also be added to the D-Flop. Lastly, I wrote a Verilog for a 32-bit wide counter. This was the main part of the project. The D-Flop’s function was to count from 1 – 256 in binary, but the problem was that the change was occurring way too fast, so the 32- bit wider counter was created to have 4 different speeds. This was simulated on the NEXYS 3 Board. If no switches were on, making the value equal 0, there was no change noticeable on the board. When the first switch was on, making the value equal 1, the LEDs were a little brighter, but still no change was visible. As the second switch was on and the first switch off, making the value equal 2, the 3 LEDs on the left were noticeably blinking, but the other 5 were still on, showing no sign of change. As both switches were turned on, making the value equal 3, the LEDs were counting from 1-256 on the board in binary. This change was very visible and every value was displayed in binary and was changing at a constant pace.